Selective area growth of III-V semiconductor nanowires and their photovoltaic and electron device applications

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We report on the systematically controlled growth of GaAs and InP and related III-V compound semiconductor nanowire arrays by catalyst-free selective area metalorganic vapor phase epitaxy on partially masked (111) oriented substrates. First, we discuss selective area growth mechanism including radial and axial growth controll [1,2]. Next, we demonstrate photovoltaic and electron device applications.

We fabricated photovoltaic devices using the core–shell pn junction InP nanowire array on the p-type InP (111)A substrates with and without AlInP window layer [3,4]. After nanowire growth, the space between nanowires was filled with a resin, and an ITO film electrode was then sputtered onto the nanowire array. The device with window layer has the short-circuit current density, J_{SC} of 23.4 mA cm^{-2}, open-circuit voltage V_{OC} of 0.457 V, and fill factor *FF* of 0.596 for an overall conversion efficiency of 6.35%, which are higher than those without window layer (3.59%). The J_{SC} of the CMS NWSCs is close to 80% that of the best InP planar solar cell reported even though their absorption volume is only 8% for the total epitaxial layer thickness of the best planar cell (3.5 micron). Similar surface passivation effect was also observed for GaAs/InGaP CMS NWSCs. Conversion efficiency improved from 0.71% to 4.01% by introducing InGaP layer [5]. We also discuss a posibility of 'flexible nanowire array' without the substrates. It is easy to remove the wire part after all the device processes, and the substrate can be reproducibly used. This flexible device has the advantage in that it needs two orders less of semiconducting materials.

Finally, we demonstrate nanowireFETs on silicon. We fabricate surrounding-gate transistors using InGaAs nanowires and InGaAs/InP/InAlAs/InGaAs core–multishell nanowires as channels. Surrounding-gate transistors using core–multishell nanowire channels with a six-sided, high-electron-mobility transistor structure greatly enhance the on-state current and transconductance while keeping good gate controllability [6]. These devices provide a route to making vertically oriented transistors for the next generation of field-effect transistors and may be useful as building blocks for wireless networks on silicon platforms. We also fabricate tunneling field-effect transistors (TFETs) using III-V nanowire/Si heterojunctions and experimentally demonstrate steep-slope switching behaviors using InAs NW/Si heterojunction TFET with surrounding-gate architecture and high-k dielectrics. Control of resistances in this device structure is important for achieving steep-slope switching. A minimum subthreshold slope (SS) of the TFET is 21 mV/dec at VDS of 0.10 – 1.00 V [7].

References

[1] K. Ikejiri, et. al., *Journal of Crystal Growth* **298** 616-619 (2007)
[2] K. Ikejiri, et. al., *Nanotechnology* **19** 26560 (2008)
[3] T. Fukui et. al. *AMBIO* **41** Suppl.2 119(2012)
[4] M. Yoshimura et. al. *APEX* **6** 052301(2013)
[5] E. Nakai, et. al. *Jpn. J. Appl. Phys.* **52** 055002(2013)
[6] K.Tomioka, et. al., *Nature* **488**, 189(2012)
[7] K.Tomioka, et. al., *Collected Abstract of VLSI Symposia* 2012