III-V Semiconductor nanowires for future devices

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Bottom-up grown semiconducting nanowires are very attractive for direct integration of III-V materials on Si thus opening up new possibilities for the design and fabrication of electronic and optoelectronic devices. In particular, the cylindrical geometry of the nanowire provides the most ideal device structure for ultimately scaled field-effect transistors (FETs) from an electrostatics perspective. Furthermore, the possibility of combining materials with high lattice mismatch in axial heterostructures makes them a first choice material for tunnel FETs (TFETs) [1]. TFETs are being considered today the most promising steep slope devices for low power applications.

In this talk we will report on our recent activities in the field of semiconducting nanowires. For the integration of III-V materials directly on silicon we have developed a new approach in which III-V homo- as well as heteroepitaxial nanowires are selectively grown within nanotube templates [2]. Hereby the morphology is defined by the shape of the template and compared to metal- or self-catalyzed nanowire growth processes the nanotube template approach does not suffer from the often observed intermixing of (hetero-) interfaces and non-intentional core-shell formation.

For the implementation of TFETs we investigate the InAs-Si system because the small effective bandgap of the heterojunction promises high tunnel currents at low voltage operation. Electrical devices require the control of doping density, which we have thoroughly studied for n-type doping of InAs nanowires. The carrier concentration and the mobility are extracted by a combination of 4-point probe measurements, Seebeck measurements and TCAD simulations [3]. We have fabricated and characterized Esaki tunnel diodes and TFETs based on InAs-Si heterostructure nanowires. High quality Esaki tunnel diodes were achieved as indicated by the negative differential resistance with a peak-to-valley current ratio of 2.44 and a tunnel current of 6 MA/cm3 at 0.5 V reverse bias. In addition, the electrical characterization of InAs-Si nanowire TFETs will be discussed [4].

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